**IBRAHIM RUPAWALA**

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Dear Sir/Madam,

I am glad to introduce myself as a graduate in Electrical and Electronics Engineering from Arizona State University, Tempe currently working as a Non Volatile Engineering Product Intern (3D NAND Flash) at Micron Technology. I am looking for opportunities in the field of Semiconductor Memories**.** I am confident that my education and experience have prepared me for the position that you have available, and my unique abilities will enable me to contribute significantly towards your objectives.

My background includes a BE degree in Electronics Engineering from Gujarat Technological University, India and MSE in Electronics and Mixed Signal Circuit Design from ASU, Tempe along with the following professional and project experiences:

* Currently working as **Non Volatile Engineering Product Intern at Micron Inc,** Milpitas, CA. Job responsibilities includes :
* Working on power and performance analysis of program and read algorithm of Micron’s B16A (64 tier TLC) NAND Flash
* Optimizing the program and read algorithm by modulating the trims to find the best settings which enables to configure the device in the best performance, least power consumption and least energy per bit modes.
* Submitting Verilog simulation jobs to analyze the waveforms for studying the circuital changes happening by triggering different trims and collecting data from the silicon to validate the behavior of the trims.
* Working with Design, Testing, Process and Manufacturing departments to recommend modifications and processes.
* Debug, design, simulation and implementation of circuit changes on production or near production products.
* Performing post - silicon validation of Micron’s 3D NAND flash using memory tester & probe - station.
* Studying advanced memory concepts like Read Window Budget (RWB), Slow Selective Program Convergence (SSPC), NAND reliability mechanisms (such as program/ read/ inhibit disturb) and studying their implication on bit error rate.
* Developed the Layout of the standard cells in 45 nm PDK and performed DRC and LVS checks as an intern at Analog Rails, Tempe, AZ
* Teaching & helping students in performing lab assignments using Cadence in the course EEE 335: Analog & Digital Circuit Design serving as a graduate teaching assistant at School of Electrical, Computer & Energy Engineering, ASU, Tempe
* Project Experience of Designing MIPS R3000 core with Data Hazard Detection, Data Forwarding, Control Hazard Detection and Branch Delay Slot in System Verilog.
* Implemented Parameterized Sequential Multiplier & Divider using Genesis2 (System Verilog and Perl).
* Advanced knowledge of Semiconductor memory design including SRAM, DRAM, Flash memories and emerging memories like RRAM and STT-RAM.
* Project Experience of RTL to GDS II Design of Lightweight Encryption (“Simon”) Engine.
* Project Experience of 16KB 8T SRAM Register File Design, Low Level D – Latch using 7 nm (FinFET) Educational PDK
* Project Experience of Designing & Simulating Standard Cell Libraries (NANDX2, NORX3 and INVX3) and 8-bit full custom modulo adder in 32 nm PDK



I thrive on new challenges and my innovative approach along with my desire to learn will prove to be an asset to my employer. I look forward to an interview to discuss with you how I can best serve your organization meet its goals.

Yours Sincerely

Ibrahim Rupawala